HA-5190
SPICE OPERATIONAL AMPLIFIER MACRO-MODEL

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Introduction

This application note describes the SPICE macro-model for the HA-5190 op amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the SPICE net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to relate the SPICE listing to the schematic. The model simulates most AC and DC parameters. The significant dominant poles and zeros are included to give the most accurate AC simulation with minimum model complexity.

Model Description

Power Supply

The supply current in the first block (1), IPS, models the typical supply current of the device. Current sourced or sinked out of the op amps output will not show up as an increase in the supply current.

Input Stage

The second block (2) of the schematic is the op amp input stage. LN, CN, LP and CP model the parasitic inductance and capacitance of the bond wires and the package. RD models the differential input resistance. RN and RP model the input transistor base resistances. CMRR, PSRR and VIO are modeled by ECR, EPR and VOF, respectively. Input bias currents are set by IBN and IBP, with the difference of the two creating the input offset current.

Gain Stage

The third block (3) models differential to single-ended conversion with gain. Voltage clamps and ES model slew rate limiting. RS and CS model the bandwith of the input stage. The diodes and voltage sources clamp the ouput voltage of this stage thereby modeling the slew rate.

Frequency Response

The fourth block (4) models the small-signal open loop frequency response. GA provides a current equal to the small signal transconductance. RH and CH model the resistance and the capacitance of the high impedance node. RC and CC2 model the compensation network.

Poles-Zeros

Section five (5) is a double pole network modeling higher order poles. EP duplicates the voltage across the compensation capacitor CC2.

Output Stage

The output stage, section six (6), includes emitter resistance, RO, and output parasitics of the bond wire inductance and package capacitance, LO and CO.

Parameters Not Modeled:

- Temperature Effects
- Differential Voltage Restrictions
- Input Noise Voltage and Current
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Power Supply Range

Spice Listing

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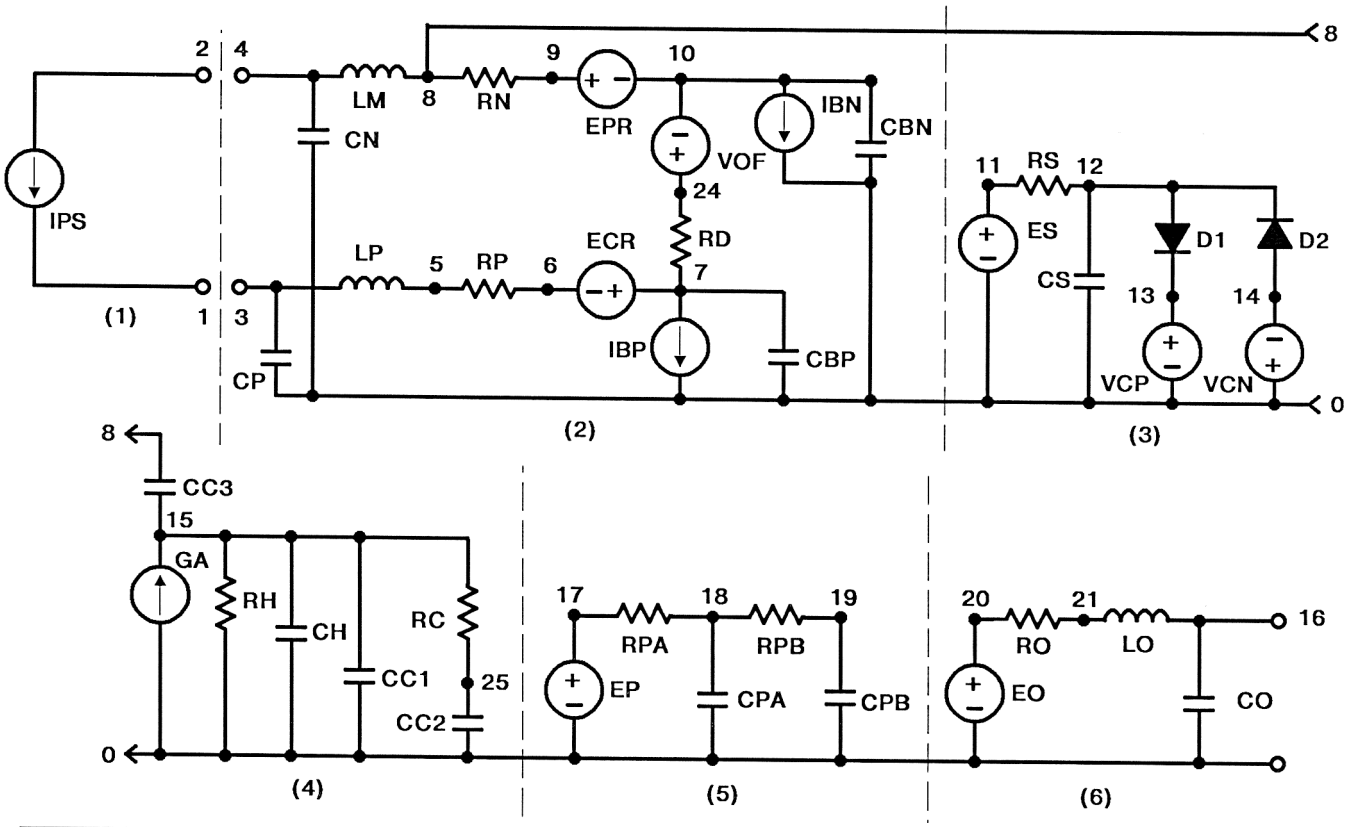
*
*HA-5190 MACRO-MODEL
*REV: 8/8/91
*BY: J. COUTREAU
*
*+IN -> NODE 3, -IN -> NODE 4, OUTPUT-> NODE 16
*V+ SUPPLY-> NODE 2, V- SUPPLY-> NODE 1
*
.SUBCKT   HA5190   3   4   2   1   16
*
*INPUT STAGE
*
LP 3 5 5E-9
RP 5 6 20
ECR 7 6 3 0 132E-6
IBP 7 0 6.7E-6
CBP 7 0 0.5E-12
LN 4 8 5E-9
RN 8 9 20
EPR 9 10 2 1 132E-6
IBN 10 0 8.3E-6
CBN 10 0 0.5E-12
RD 7 24 28.8E3
VOF 24 10 2E-3
*
*SLEW LIMITING
*
ES 11 0 7 24 10
RS 11 12 100
CS 12 0 9E-12
D1 12 13 DM OFF
D2 14 12 DM OFF
.MODEL DM D (IS=1E-9 BV=40 IBV=50E-6)
VCP 13 0 1.2
VCN 0 14 1.2
*
*FREQUENCY RESPONSE
*
GA 0 15 12 0 1.43E-3
RH 15 0 2E6
CH 15 0 3E-12
CC1 15 0 6E-12
RC 15 25 1E3
CC2 25 0 1.8E-12
CC3 15 8 1.5E-12
*
*POLES
*
EP 17 0 25 0 1
RPA 17 18 75
CPA 18 0 7E-12
RPB 18 19 75
CPB 19 0 7E-12
*
*OUTPUT STAGE
*
EO 20 0 19 0 1
RO 20 21 25
LO 21 16 5E-9
CO 16 0 2E-12
*
*POWER SUPPLY CURRENT
*
IPS 2 1 19E-3
*
.ENDS HA5190
```

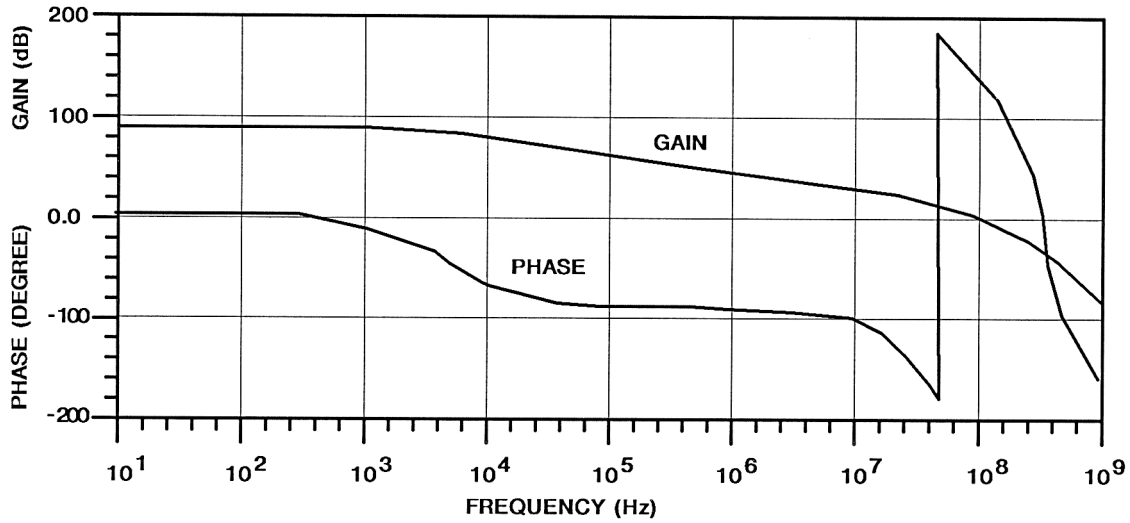
Macro-Model Schematic



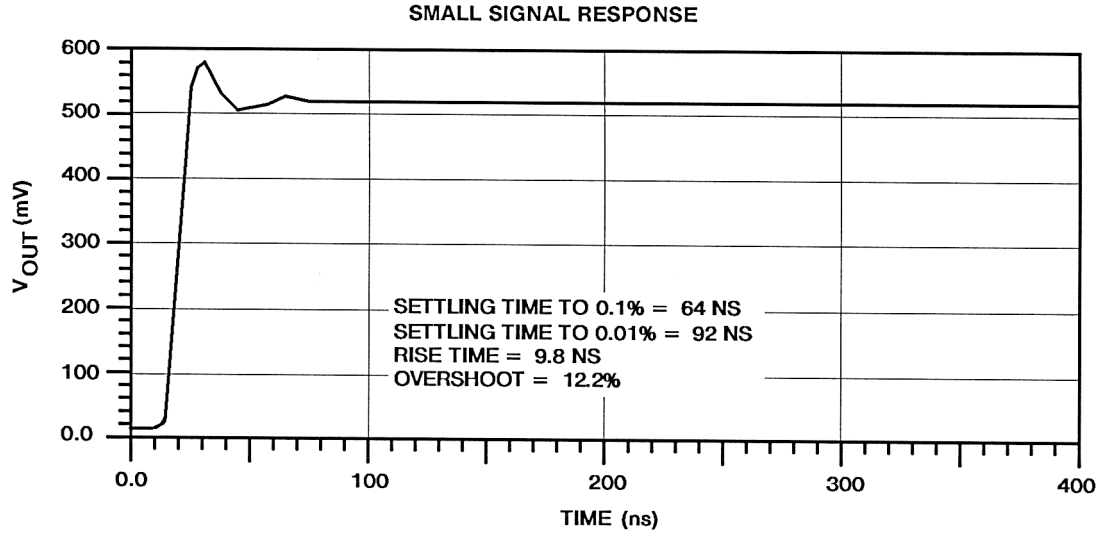
Model Performance

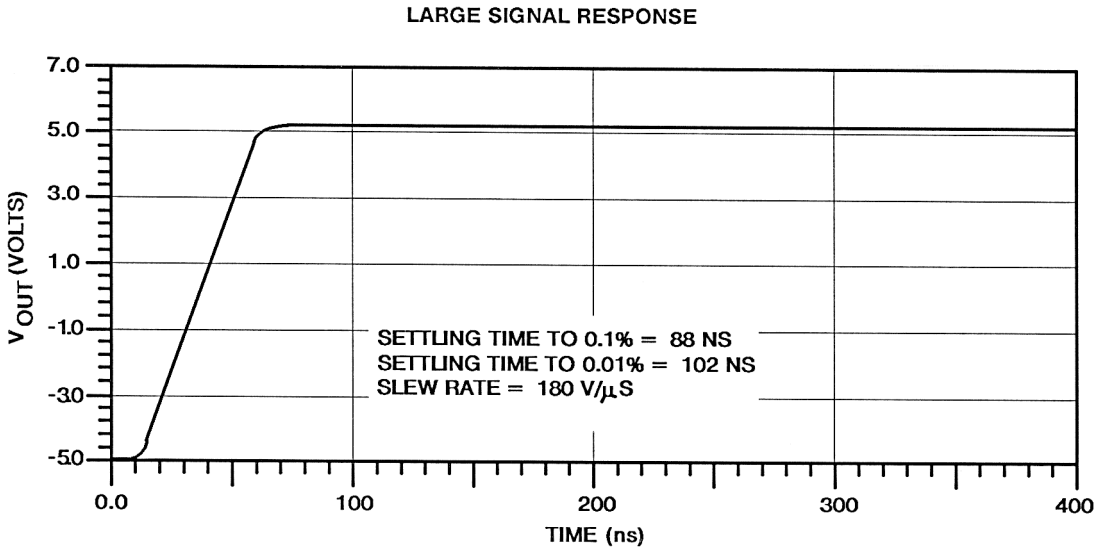
Conditions: V_{SS} = ±15V, A_{VCL} = +5, Unless Otherwise Specified

OPEN LOOP GAIN AND PHASE PLOT



Model Performance (Continued)





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